UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/497,320	02/03/2000	Ahmad Ghaemmaghami	E0545/1516P	7350

7590 10/04/2005

KELLY K, KORDZIK, WINSEAD SECHREST & MINICK P.C.
5400 RENAISSANCE TOWER
1201 ELM STREET
DALLAS, TX 75270

EXAMINER	
DIAZ, JOSE R	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/497,320
Filing Date: February 03, 2000
Appellant(s): GHAEMMAGHAMI ET AL.

Robert A. Voigt, Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 6, 2005 appealing from the Office action mailed June 3, 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

US Pat. No. 5,320,974	Hori et al.	Fig. 3.
US Pat. No. 6,051,458	Liang et al.	Fig. 1C.
US Pat. No. 6,037,107	Thackeray et al.	Col. 1, ll. 35-38.
US Pat. No. 6,020,244	Thompson et al.	Col. 3, ll. 18-19.
US Pat. No. 6,352,903 B1	Rovedo et al.	Col. 1, ll. 49-55; figs. 2A-2B
Wolf et al., "Silicon Processing for the VLSI Era: Volume 1-Process Technology", Lattice Press, 1986.		Fig. 36(b) on page 322
Kang et al., "CMOS Digital Integrated Circuits: Analysis and Design", 2nd ed., McGraw-Hill, 1999.		Fig. 2.6 on page 31

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 4-5, 8, and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori et al. (US Pat. No. 5,320,974) in view of Wolf et al. ("Silicon Processing for the VLSI Era, Volume 1-Process Technology", Lattice Press, 1986, pp. 321-324), previously cited in the Office action mailed on May 6, 2003.

Regarding claims 1 and 8, Hori et al. teach a method for providing a halo implant in a semiconductor device comprising the steps of:

(a) providing a thin mask layer (MASK) to the semiconductor device (N + POLY-Si GATE) that covers a substantial amount of an active area comprising a drain region (DRAIN REGION) (see figs. 3-4)[1]; and

(b) providing the halo implant (B+) (see fig. 3).

However, Hori et al. fails to teach a mask layer comprising photoresist. Wolf et al. teaches that it is well known in the art to use photoresist in place of SiO_2 as a mask. (see last paragraph of page 321 of Wolf et al.).

Hori et al. and Wolf et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use photoresist instead of a metal or an oxide film as the ion implantation mask material. The motivation for doing so, as is taught by Wolf et al., is that photoresist have good ion stopping power in the smallest thickness (see last paragraph of page 321 of Wolf et al.). Therefore, it would have been obvious to combine Wolf et al. with Hori et al. to obtain the invention of claims 1, 4, 5, 8, 11 and 12.

Regarding claims 4 and 11, Hori et al. teach that a halo implant angle of about 45° (see col. 6, lines 60-63).

Regarding claims 5 and 12, Hori et al. teach providing LDD regions (6a and 6b) (see Figs. 1A and 2C) before the halo implant (B+) (see figs. 1C).

---

[1] With regards to the limitation that the mask layer covers a substantial amount of an active area comprising a source region, it is noted that figures 3 and 4 show an enlarged sectional view of the drain structure (7b) of the MOS transistor disclosed in figures 1C and 2A-2C, in which the mask layer (8a and 8b) is also shown covering the source region (7a). In addition, Hori et al. teaches the use of SiO_2 instead of $TiSi_2$ as the mask layer (8a and 8b) (See col. 7, lines 44-46, and figures 3 and 4).

Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori et al. (US Pat. No. 5,320,974) in view of Wolf et al. ("Silicon Processing for the VLSI Era, Volume 1-Process Technology", Lattice Press, 1986, pp. 321-324), and further in view of Thackeray et al. (US Pat. No. 6,037,107).

Regarding claims 7 and 14, a further difference between the prior art and the claimed invention is the use of DUV. Thackeray et al. teaches that it is well known in the art to expose the photoresist mask to deep ultraviolet (DUV) radiation (see col. 1, lines 35-38).

Hori et al., Wolf et al. and Thackeray et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to expose the photoresist mask to deep ultraviolet (DUV) radiation. The motivation for further doing so, as is taught by Thackeray et al., is that DUV exposure provides patterns of reduced feature size (see col. 1, lines 35-38). Therefore, it would have been obvious to further combine Thackeray et al. with Hori et al. and Wolf et al. to obtain the invention of claims 7 and 14.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liang et al. (US Pat. No. 6,051,458) in view of Wolf et al. ("Silicon Processing for the VLSI Era, Volume 1-Process Technology", Lattice Press, 1986, pp. 321-324).

Regarding claim 18, Liang et al. teaches a device comprising:

a gate (22A) (see fig. 1C);

an oxide trench (14A and 14B) (see fig. 1C);

a drain region (24D) adjacent to said oxide trench (14B) (see fig. 1C);

a source region (24S) adjacent to said oxide trench (14A) (see fig. 1C), and

a photoresist layer (PR2) over said oxide trench (14A and 14B) and over a substantial portion of said source (24S) and said drain (24D) regions, wherein a halo implant (26') is implanted using said photoresist layer (PR2) and said gate (22A) as a mask (see fig. 1C). Furthermore, Liang et al. teaches that the boron ions (26') are implanted at energy from about 15keV to about 50 keV (see col. 3, lines 35-37).

However, Liang et al. fails to teach a photoresist layer of a thickness between 0.1-0.2 μm.

Wolf et al. teaches that it is well known in the art to implant boron ions by using a thin photoresist of, for example, 0.2 μm (Please note that figure 36b of Wolf shows minimum thickness of a photoresist material required to stop 99.99% of incident ions as a function of energy and of ionic type. For example, a photoresist of about 0.2 μm is required for stopping boron ions implanted at an energy of about 30 keV).

Liang et al. and Wolf et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a thin photoresist of about 0.2 μm. The motivation for doing so, as is taught by Wolf et al., is to restrict the ionic species from being implanted into unwanted substrate regions (see last paragraph of page 321 of Wolf et al.). Therefore, it would have been obvious to combine Wolf et al. with Liang et al. to obtain the invention of claim 18.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liang et al. (US Pat. No. 6,051,458) in view of Wolf et al. ("Silicon Processing for the VLSI Era, Volume 1-Process Technology", Lattice Press, 1986, pp. 321-324), and further in view of Thompson et al. (US Pat. No. 6,020,244).

Regarding claim 19, a further difference between the prior art and the claimed invention is implanting the halo implant at an angle of about 45 degree.

Thompson et al. teaches that it is well known in the art to implant at an angle of 45 degree (see col. 3, lines 18-19).

Thompson et al., Liang et al. and Wolf et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further implanting the halo species at an angle of 45 degree. The motivation for further doing so, as is taught by Thompson et al., is improving punchthrough characteristics (col. 1, lines 40-41). Therefore, it would have been obvious to combine Thompson et al. with Wolf et al. and Liang et al. to obtain the invention of claim 19.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liang et al. (US Pat. No. 6,051,458) in view of Wolf et al. ("Silicon Processing for the VLSI Era, Volume 1-Process Technology", Lattice Press, 1986, pp. 321-324), and further in view of Thackeray et al. (US Pat. No. 6,037,107)

Regarding claim 20, a further difference between the prior art and the claimed invention is the use of DUV layer. Thackeray et al. teaches that it is well known in the art to expose the photoresist mask to deep ultraviolet (DUV) radiation (see col. 1, lines 35-38).

Liang et al., Wolf et al. and Thackeray et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further expose the photoresist mask to deep ultraviolet (DUV) radiation. The motivation for further doing so, as is taught by Thackeray et al., is to effectively activate the photoactive component of the photoresist system (see col. 12, lines 60-62 and col. 13, lines 1-6). Therefore, it would have been obvious to further combine Thackeray et al. with Liang et al. and Wolf et al. to obtain the invention of claim 20.

(10) Response to Argument

A. The rejection of claims 1, 4-5, 8 and 11-12 under 35 U.S.C. §103(a) as being unpatentable over Hori in view of Wolf.

Appellant's arguments have been fully considered but they are not persuasive. Appellant begins by arguing that Hori teaches an embodiment using a titanium silicide mask **8a** and **8b**, which has an ion stopping power of about 1.5 times higher than of silicon that does not allow boron ions to permeate near pn-junctions between the n+-type source and drain regions **7a** and **7b** and the substrate [Appellant's brief, page 5].

However, this argument seems to show instead that Appellant has misinterpreted or misread the rejection. It is conceded that Hori discloses an embodiment using titanium silicide as a mask [Hori, column 6, ll. 55-56]. However, Hori also teaches the use of silicon oxide as alternate material for said mask [Hori, fig. 3 and col. 7, ll. 45-46], which the rejection is based upon. Hence, Appellant's arguments toward the use of titanium silicide are without merit as this was not the basis of the rejection.

Appellant next discusses the teachings of Wolf and argued that the examiner has not provided any evidence that would suggest that a photoresist, with the same thickness as titanium silicide, would have an ion stopping power similar to titanium silicide [Appellant's brief, page 5]. Again, as pointed above, this argument misunderstands the rejection. Hori teaches the use of silicon oxide as a mask [Hori, fig. 3 and col. 7, ll. 45-46]. Wolf teaches that photoresist is a known material substitute for silicon oxide (SiO_2) [Wolf, page 321], and further provides two graphs [figs. 36(a) and 36(b)] teaching ion implantation energy versus thickness for silicon oxide and photoresist, respectively. As taught by Wolf, both silicon oxide and photoresist have the ability to stop 99.99% of ionic species for a given thickness (which thickness are within the range as later recited in the claims). In all, a comparison of titanium silicide and photoresist is not necessary.

On page 7 of the brief, Appellant argues that the examiner fails to provide a comparison between the silicon oxide and the photoresist. However, this argument ignores the express teaching of Wolf. For instance, figures 36(a) and 36(b) of Wolf teaches ion implantation energy versus thickness for silicon oxide and photoresist,

respectively. As taught by Wolf, both silicon oxide and photoresist have the ability to stop 99.99% of ionic species for a given thickness. As such, a comparison between the silicon oxide and the photoresist has been provided.

In addition, Appellant argues that Wolf destroys the principle of operation in Hori since the thickness of the photoresist must be greater than the thickness of silicon oxide, and consequently, the angle at which the boron ions would have to be implanted into the substrate would have to steeper than 25 to 45 degrees [Appellant's brief, pages 8-9]. However, the examiner disagrees. Hori teaches that boron ions are implanted at 30 to 50 keV [Hori, col.6, ll. 53-54]. As such energy, it is conceded that Wolf teaches a photoresist layer having a thickness which is greater than the thickness of a silicon oxide [see figs. 36(a) and 36(b)]. However, it is further noted that Wolf, at an energy of 30 keV, teaches a photoresist thickness of about 0.2 μm, which is the same thickness disclosed by Appellant [claim 18 and Appellant's Specification, page 4, last paragraph]. As such, the function of Hori will not change as a result of the combination since Wolf teaches the use of a thin photoresist which falls within the range disclosed by Appellant, which results in the formation of the claimed halo regions.

B. The rejection of claims 7 and 14 under 35 U.S.C. §103(a) as being unpatentable over Hori in view of Wolf, and further in view of Thackeray.

Turning now to the rejection of claims 7 and 14, it is noted that Appellant merely reasserts the previous argument that Hori teaches the use of titanium silicide as a mask

[Appellant's brief, pages 9-14] and thus, by combining Hori with Wolf and further with Thackeray, "the principle of operation in Hori would change, and subsequently render the operation of Hori to perform its purpose unsatisfactorily." [Appellant's brief, page 12]. Again, and for the same reasons given in the preceding paragraphs, Appellant's arguments are flawed and must fail because Appellant is arguing a rejection that was not made.

C. The rejection of claim 18 under 35 U.S.C. §103(a) as being unpatentable over Liang in view of Wolf.

Appellant next discussed the rejection of claim 18 by arguing that Wolf destroys the principle of operation in Liang since "Wolf illustrates that the thickness of the photoresist to stop 99.99% of the boron ions at an energy from about 15 keV to about 50keV (implant energy cited by Liang) requires a thickness much greater than 0.2 μm." [Appellant's brief, page 15]. However, the examiner disagrees. Liang, as acknowledged by Appellant, teaches that boron ions are implanted at about 15 to 50 keV [Liang, col. 3, ll. 36-37]. It is conceded that Wolf requires a thicker photoresist at energy of 50 keV [fig. 36(b)]. However, it also noted that Wolf requires a photoresist of about 0.2 μm or thinner (which is within the claimed range) when the boron ions are implanted at energy of 30 keV or less [fig. 36(b)]. It has been held that in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a *prima facie* case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). As such, the function of

Hori will not change as a result of the combination since Wolf teaches the use of a thin photoresist which falls within the range disclosed by Appellant.

Appellant continues by arguing that neither Liang nor Wolf teach "an oxide trench where a drain region and a source region are adjacent to that oxide trench." [Appellant's brief, page 16]. However, the examiner disagrees. Liang, as stated in the rejection, teaches an oxide trench **14A** and **14B** [fig. 1C]. As is known in the art, the reference signs **14A** and **14B** do not show two separate oxide trenches as argued, but merely show portions of the same oxide trench which is formed surrounding the transistor area [see trench isolation region **210** in US 6,352,903 B1 to Rovedo et al., col. 1, lines 49-55 and figures 2A-2B; and SiO_2 region in Kang et al., "CMOS Digital Integrated Circuits: Analysis and Design", 2nd ed., McGraw-Hill, 1999, figure 2.6]. Thus, the drain region and the source region are formed adjacent to the same oxide trench.

In addition, Appellant argues that Liang fails to teach a photoresist over the oxide trench and over a substantial portion of the source and drain regions, as recited in claim 18 [Appellant's brief, pages 16-17]. However, this argument ignores the express teaching of Liang. Liang, as stated in the rejection, teaches a photoresist (**PR2**) which is formed over portions of the source and drain regions (**24S** and **24D**) and the trench oxide (**14A, 14B**) [fig. 1C].[2] With regards to the limitation that the photoresist is over a "substantial portion" of the source and drain regions, the court has held that the term "substantial" is a meaningful modifier implying "approximate," rather than "perfect". *Playtex Products Inc. v. Procter & Gamble Co.*, 73 USPQ2d 2010 (CAFC 2005) citing

Liquid Dynamics Corp. v. Vaughan Co., Inc., 69 USPQ2d 1595 (CA FC 2004). Thus, the term "substantial" is merely a term of degree and should not be interpreted as having a strict numerical limitation. As such, the regions covered with photoresist (PR2) can be considered to be "substantial" in light of the previously cited case.

D. The rejection of claim 19 under 35 U.S.C. §103(a) as being unpatentable over Liang in view of Wolf and further in view of Thompson.

Appellant next turns to the obviousness rejection over Liang in view of Wolf and further in view of Thompson [Appellant's brief, pages 17-22]. The rejection over Thompson was made based on Appellant's limitation that the halo implant is implanted at a "substantially 45 degree angle." The reference Thompson was cited merely to show that it is known in the art to implant impurities as such an angle. In fact, this teaching is also disclosed in column 6, lines 60-62 of the previously cited reference Hori et al. Thus, the fact that Thompson formed region (**25**) [fig. 2] instead of the conventional halo region (**15,16**) [fig. 1], as argued by Appellant, is irrelevant since the sole purpose of citing Thompson is to demonstrate that the claimed implantation angle of 45 degrees is known in the art. As such, the argument is not persuasive.

---

[2] As noted above, the reference signs **14A** and **14B** do not show two separate oxide trenches, but merely show portions of the same oxide trench which is formed surrounding the transistor area.

E. The rejection of claim 20 under 35 U.S.C. §103(a) as being unpatentable over Liang in view of Wolf and further in view of Thackeray.

As to the rejection of claim 20, Appellant argues that "the Examiner's motivation is insufficient to support a prima facie case of obviousness for rejecting claim 20" [Appellant's brief, pages 22-24]. The court has held that as long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor. *In re Beattie*, 24 USPQ2d 1040 (Fed. Cir. 1992) citing *In re Kronig*, 539 F.2d 1300, 1304, 190 USPQ 425, 427-28 (CCPA 1976) and *In re Lintner*, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972). In the instance case, Thackeray teaches the motivation in column 12, ll. 60-65: "to effectively activate the photoactive component of the photoresist system...to produce a patterned image." As such, the rejection is considered to be proper.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

9/27/05

José R. Díaz
Examiner- Art Unit 2815

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Tom Thomas
SPE- Art Unit 2815

Darren E. Schuberg
SPE- Art Unit 2834

second edition

CMOS DIGITAL INTEGRATED CIRCUITS

Analysis and Design

SUNG-MO (STEVE) KANG
University of Illinois at Urbana- Champaign

YUSUF LEBLEBICI
Worcester Polytechnic Institute
Swiss Federal Institute of Technology-Lausanne

WCB McGraw-Hill

Boston Burr Ridge, IL Dubuque, IA Madison, WI New York San Francisco St. Louis
Bangkok Bogotá Caracas Lisbon London Madrid
Mexico City Milan New Delhi Seoul Singapore Sydney Taipei Toronto

WCB/McGraw-Hill

A Division of The McGraw-Hill Companies

To Myoung-A, Jennifer and Jeffrey,
and Anıl and Ebru

CMOS DIGITAL INTEGRATED CIRCUITS: ANALYSIS AND DESIGN

This book is printed on acid-free paper.

3 4 5 6 7 8 9 0 DOC/DOC 9 3 2 1 0 9

ISBN 0-07-292507-8

Vice president and editorial director: Kevin T. Kane
Publisher: Thomas Casson
Executive editor: Elizabeth A. Jones
Senior developmental editor: Kelley Butcher
Marketing manager: John T. Wannemacher
Project manager: Karen Nelson
Senior production supervisor: Heather D. Burbridge
Senior designer: Lorna Lo
Cover designer: Nicole Leong
Supplement coordinator: Linda Huenecke
Typeface: 10/12 Times Roman
Printer: R. R. Donnelley & Sons Company

Library of Congress Cataloging-in-Publication Data

Kang, Sung Mo, (date)
CMOS digital integrated circuits: analysis and design/Sung-Mo (Steve) Kang, Yusuf Leblebici.
–2nd ed.
p. cm.
Includes index.
ISBN 0-07-292507-8
1. Metal oxide semiconductors, Complementary. 2. Digital integrated circuits. I. Leblebici, Yusuf.
II. Title.
TK7871.99M44K36 1999
621.39'5--dc21 98-28075

http://www.mhhe.com

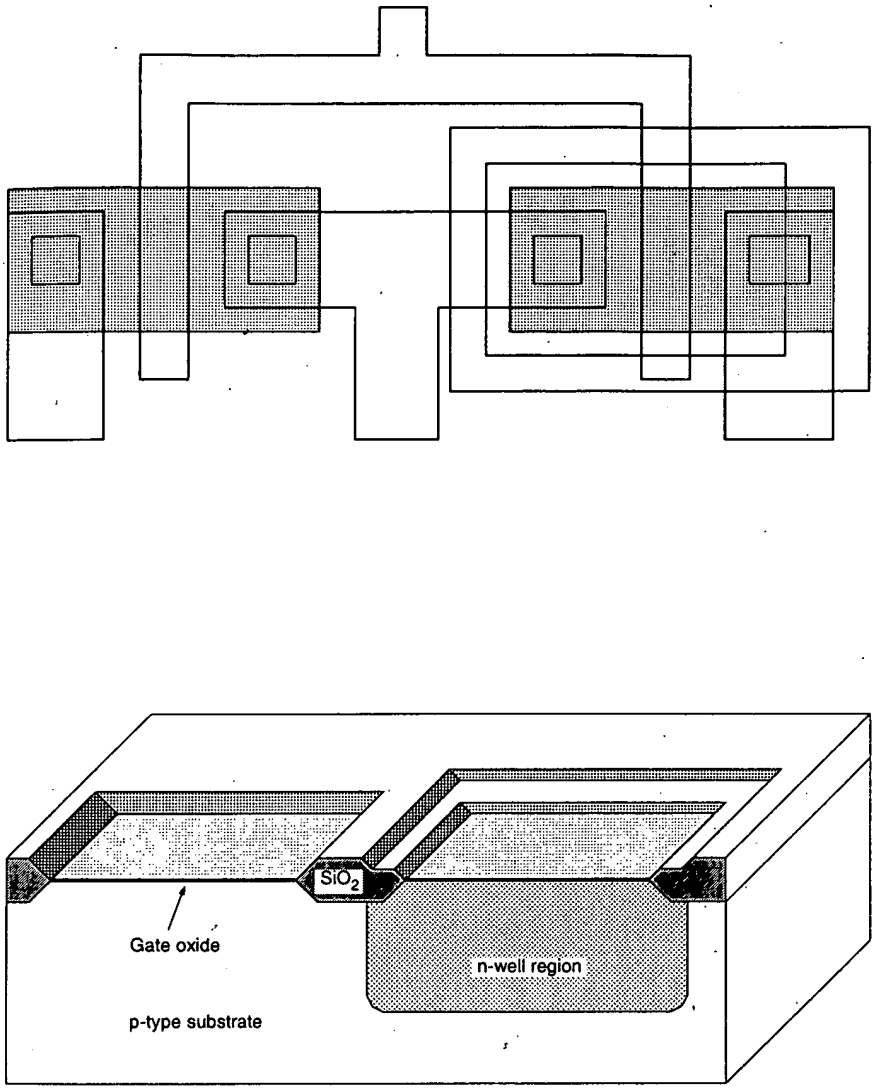


Figure 2.6. Following the creation of the n-well region, a thick field oxide is grown in the areas surrounding the transistor's active regions, and a thin gate oxide is grown on top of the active regions. The thickness and the quality of the gate oxide are two of the most critical fabrication parameters, since they strongly affect the operational characteristics of the MOS transistor, as well as its long-term reliability. After *Atlas of IC Technologies*, by W. Maly [1].

US006352903B1

(12) **United States Patent**
Rovedo et al.

(10) **Patent No.: US 6,352,903 B1**
(45) **Date of Patent: Mar. 5, 2002**

(54) **JUNCTION ISOLATION**

(75) Inventors: **Nivo Rovedo**, LaGrangeville; **David B. Colavito**, Rock Hill, both of NY (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 56 days.

(21) Appl. No.: **09/605,730**

(22) Filed: **Jun. 28, 2000**

(51) **Int. Cl.**[7] **H01L 21/20**
(52) **U.S. Cl.** **438/387**; 438/240; 438/396
(58) **Field of Search** 257/382, 384, 257/412, 413, 388, 377; 438/424, 255, 253, 595, 242, 239, 254, 240, 387, 396, 256

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,316,982 A * 5/1994 Matsuo et al.
5,976,928 A * 11/1999 Kirin et al. 428/240
6,030,867 A * 2/2000 Chien et al. 438/255
6,184,078 B1 * 2/2001 Yoon et al. 438/253
6,200,854 B1 * 4/2001 Chuang 438/253
6,235,575 B1 * 5/2001 Kasai et al. 438/242

FOREIGN PATENT DOCUMENTS

JP 2000195967 A * 7/2000 ..... H01L/21/8234

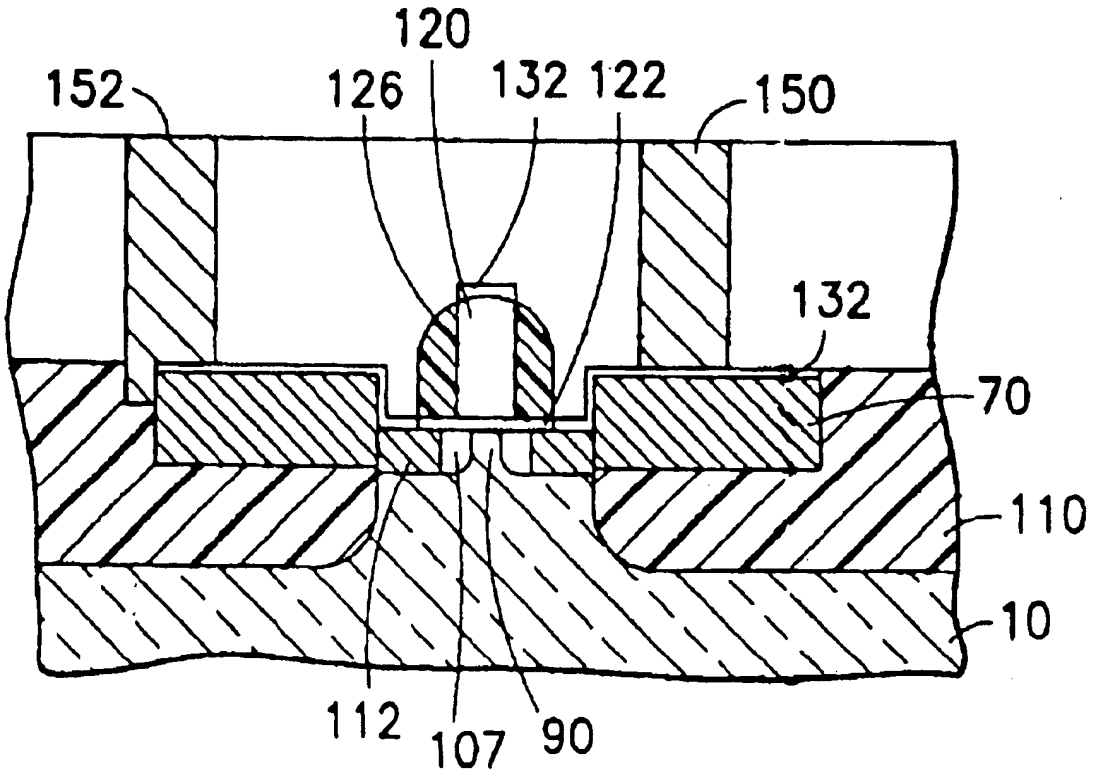
* cited by examiner

Primary Examiner—Matthew Smith
Assistant Examiner—V. Yevsikov
(74) *Attorney, Agent, or Firm*—Eric W. Petraske

(57) **ABSTRACT**

In a bulk silicon process, an insulating layer is placed under the portion of the source and drain used for contacts, thereby reducing junction capacitance. The processing involves a smaller than usual transistor area that is not large enough to hold the contacts, which are placed in an aperture cut into the shallow trench isolation.

6 Claims, 2 Drawing Sheets



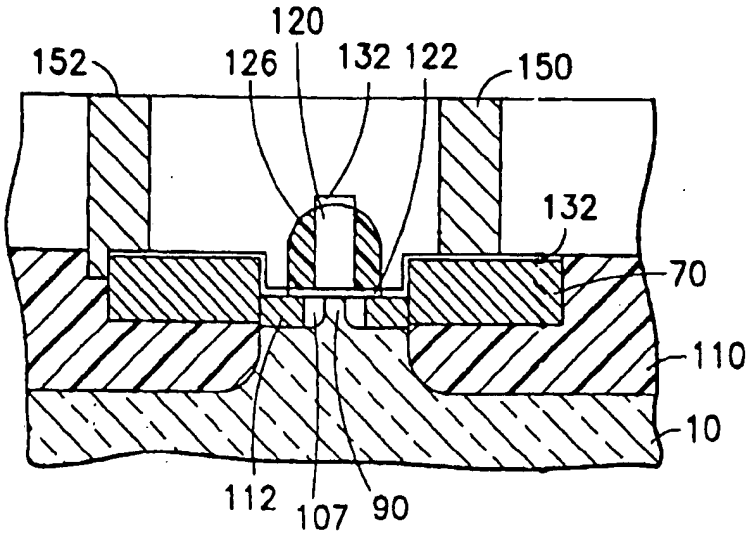


FIG.1

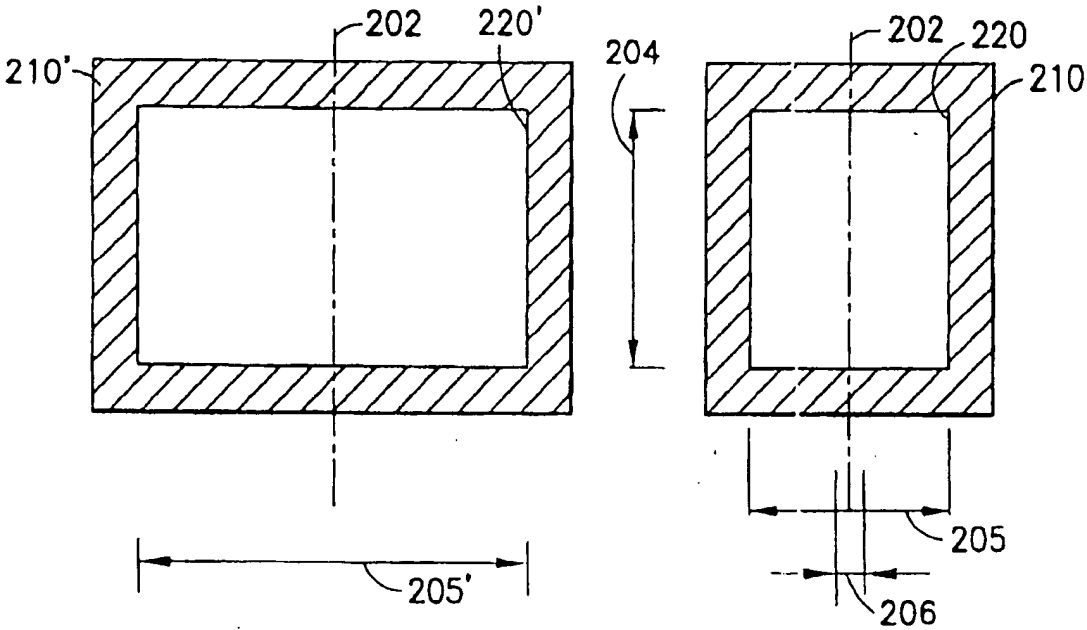


FIG.2A
PRIOR ART

FIG.2B

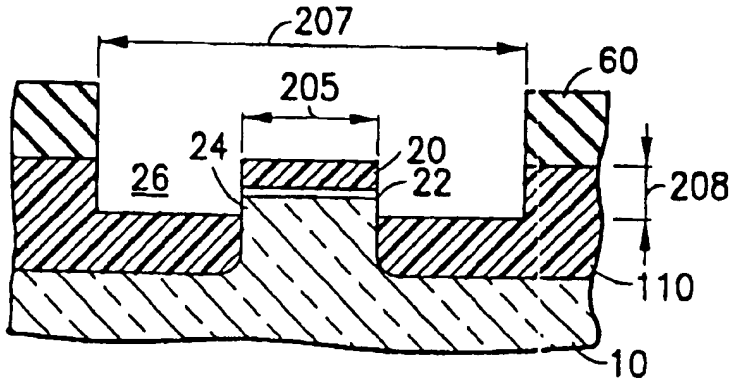


FIG.3

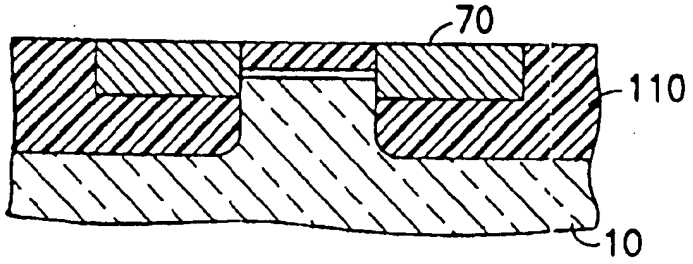


FIG.4

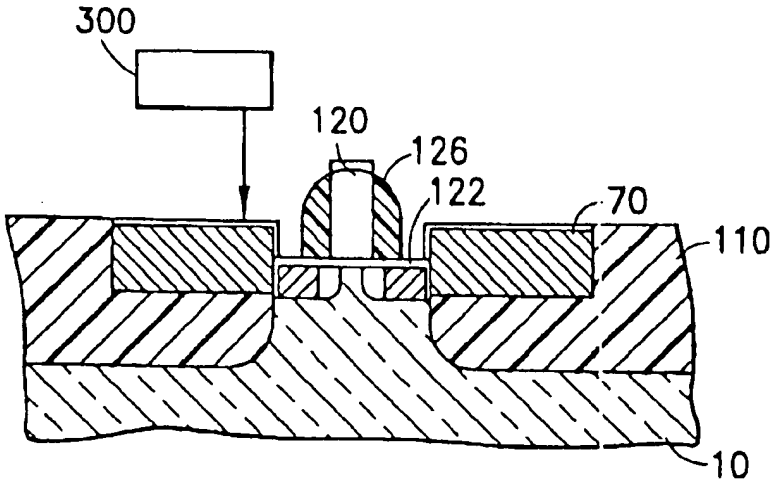


FIG.5

JUNCTION ISOLATION

FIELD OF THE INVENTION

The field of the invention is integrated circuit processing, in particular low-capacitance high speed circuits.

BACKGROUND OF THE INVENTION

It is well known in the field that junction capacitance between sources and drains (S/D) and the substrate is an important limiting factor in circuit performance. In addition, S/D to substrate leakage results in useless power consumption. Furthermore, contacts to SID diffusions may suffer form reliability concerns if the etch of the contacts places the conductive material of the contact in close proximity to the bottom junction edge through overetch or misalignment.

Silicon on insulator technology has less junction capacitance than bulk technology because the buried insulator reduces the capacitance, but is more expensive.

It is desirable to develop a low-capacitance transistor structure with low SID leakage for bulk silicon integrated circuits that is economical to manufacture.

SUMMARY OF THE INVENTION

A feature of the invention is the formation of conductive contact pads over a portion of the STI to reduce the area, reduce capacitance and leakage between the source/drain and the silicon substrate.

Another feature of the invention is a reduced size of the transistor area within the shallow trench isolation (STI) that is less than would have been required to provide space for contacts to the rest of the circuit if these contacts were fully within the active region.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows in cross section a completed transistor constructed according to the invention.

FIG. **2A** shows a top view of a prior art transistor area.

FIG. **2B** shows a top view of a transistor area according to the invention.

FIGS. **3–5** show in cross section various steps in practicing the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. **2A** shows a top view of a prior art transistor area after the step of forming the shallow trench isolation **210'** (STI), in which area **220'** which will hold the transistor gate (centered on axis **202**), source and drain, is defined by trench **210'**, illustratively formed in a conventional etching process, filled with oxide and planarized in a chemical-mechanical polishing step (CMP). FIG. **2B** shows a corresponding view of area **220** according to the invention bounded by STI **210**. Note that the length. **204** along the gate is the same but that area **220** is much smaller than area **220'** in the prior art. As will be described later, the area for the sources and drains is reduced below what is required for contacts to fit. The phrase "reduced source and drain areas" will be used in the claims to mean that the source and drain in the single-crystal substrate are too small to receive contacts in the ground rules in use in that particular process. Arrow **206** denotes the width of the gate to be formed and arrow **205** denotes the width of the gate sidewalls plus a small margin for manufacturing tolerance. Illustratively, in a 0.18 μm ground rule CMOS process, gate width **206** is 0.18 μm and width **205** is 0.49 μm. Contacts illustratively require a contact area of 0.46 μm×0.46 μm including manufacturing tolerance, so total active area width **205'** would be 1.1 μm, compared to about 1 μm in the contact pads.

Referring now to FIG. **3**, there is shown in cross section the portion of the circuit that will hold an illustrative transistor. Substrate **10** has been prepared by forming a conventional pad oxide (SiO_2) **22** and pad etch stop layer **20**, illustratively nitride (Si_3N_4). STI member **110** has been etched in a conventional process using C_4F_8 chemistry chemistry selective to nitride to form recess **26** having a contact pad depth denoted by arrow **208**. Resist **60** has been patterned with a noncritical contact etch aperture having a width denoted by arrow **207**. The contact recess apertures **26** define contact portions of the STI member **110** that will contain contact pads for interconnects to make contact with the source and drain. If the ground rules would be violated by placing contacts on the STI, then appropriate corrections will be made, such as increasing the width of the STI or spacing adjacent elements further away. The contact pad depth of aperture **26** is such that the vertical contact surface **24** that will be the electrical contact between the source/drain and the contact pads is sufficiently large. Illustratively the depth of the recess is 0.2 μm and the vertical contact surface is 0.08 μm high.

Referring now to FIG. **4**, there is shown the same area after the deposition of conductive material **70** and CMP using the pad nitride **20** and STI **110** as a polish stop. Illustratively, the conductive material is polycrystalline silicon or amorphous silicon.

Next, as shown in FIG. **5**, pad nitride **20** is stripped, wells are formed, pad oxide **22** is stripped, gate oxide **122** is grown, gate stack **120** is formed and patterned, the low dose implant is performed in the source/drain areas **122**, gate sidewalls **126** are formed, the source/drain and contact pads are implanted, and an activation anneal is performed. The circuit is completed by forming conventional interconnection members and interlayer dielectrics, denoted schematically by a box labeled **300**.

FIG. **1** shows the final structure, in which contact pads **70** bracket the transistor, comprising gate **120** and gate oxide **122**, with sidewalls **126** and gate silicide **132**. Silicide **132** is also formed on top of contact pads **70**. Beneath the gate, source/drain **112** is implanted at the same time as the contact pads. As can be seen, the portion of the S/D members extending outwardly past the sidewalls is only a manufacturing tolerance and not enough to hold a contact. S/D members of this size will be referred to in the claims as "reduced S/D members". A conventional lower dose source/drain extension has been formed. Contact interconnect members **150** and **152** are shown. Contact **152** illustrates an advantageous feature of the invention—if the contact is misaligned so that it partly lands on the STI, no harm is done. The contact etch will merely penetrate into the STI, with additional contact area being formed on the vertical wall of the contact pad. Note that contact pad members **70** can be extended over an STI member to form a local interconnect between the diffusions on either side of that STI member.

While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims. By way of example, the substrate may be silicon or silicon-germanium; the gate dielectric may be thermal oxide or a high-k material such as N_2O_3 or silicon nitride; the planariz-

ing step may be performed by etching instead of CMP; the conductive material may be polycrystalline silicon, amorphous silicon, SiGe, etc. The substrate is not necessarily bulk silicon. The invention may be performed in SiGe, or in an SOI substrate if the thickness of the silicon device layer is thick enough to give rise to significant capacitance, or if the thickness of the insulating layer is thin enough to give rise to significant capacitance.

We claim:

1. A method of forming an integrated circuit in a semiconductor substrate comprising the steps of:

preparing said substrate, including forming a pad etch stop layer;

forming a set of STI members defining a set of transistor areas covered by said pad etch stop, said transistor areas having reduced source and drain areas;

defining a set of contact etch apertures in a resist area, said contact etch apertures covering said transistor areas and extending over a contact portion of said STI members on opposite sides of said transistor areas;

etching said contact portion of said STI members to a contact pad depth in a contact pad aperture, thereby exposing vertical contact surfaces in said substrate on said opposite sides of said transistor region;

depositing a layer of conductive material, thereby forming contact pads in said contact pad apertures, said contact pads being in electrical contact with said vertical contact surfaces;

forming transistors in said transistor areas, said transistors having sources and drains contacting said contact pads through said vertical contact surfaces; and

forming a set of interconnection members to complete said integrated circuit, at least some of said interconnection members contacting said contact pads.

2. A method according to claim 1, in which said reduced source and drain areas have dimensions less than are required to hold contacts.

3. A method according to claim 2, in which said step of etching said contact portion of said STI members is performed with an etchant selective to said etch stop layer, whereby said etch stop layer protects said transistor area thereunder.

4. A method according to claim 2, in which said pad etch stop layer is formed from nitride, said STI members are formed from oxide and said conductive material is silicon.

5. A method according to claim 1, in which said step of etching said contact portion of said STI members is performed with an etchant selective to said etch stop layer, whereby said etch stop layer protects said transistor area thereunder.

6. A method according to claim 5, in which said pad etch stop layer is formed from nitride, said STI members are formed from oxide and said conductive material is silicon.

* * * * *